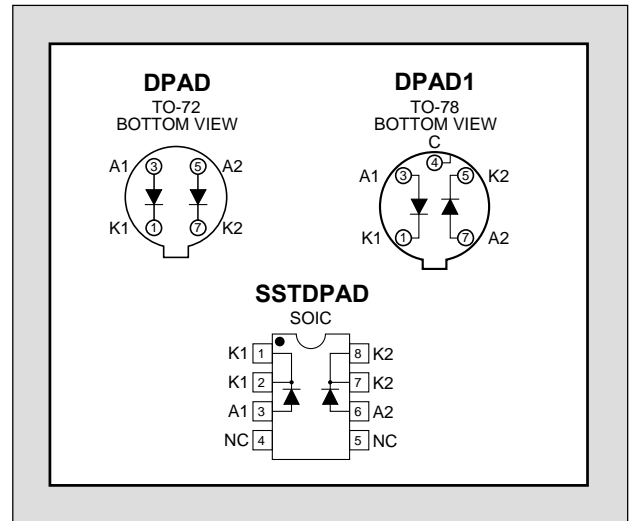


DPAD SERIES

MONOLITHIC DUAL PICO AMPERE DIODES

| FEATURES | |
|--|--------------------------------|
| Direct Replacement For SILICONIX DPAD SERIES | |
| HIGH ON ISOLATION | 20fA |
| EXCELLENT CAPACITANCE MATCHING | $\Delta C_R \leq 0.2\text{pF}$ |
| ABSOLUTE MAXIMUM RATINGS¹ | |
| @ 25 °C (unless otherwise stated) | |
| Maximum Temperatures | |
| Storage Temperature | -65 to +150 °C |
| Operating Junction Temperature | -55 to +135 °C |
| Maximum Power Dissipation | |
| Continuous Power Dissipation (DPAD) | 500mW |
| Maximum Currents | |
| Forward Current (DPAD) | 50mA |



COMMON ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

| SYMBOL | CHARACTERISTIC | MIN | TYP | MAX | UNITS | CONDITIONS |
|-------------------|---|----------------------|-----|-----|-------|---|
| BV_R | Reverse Breakdown Voltage | DPAD1 | -45 | | V | $I_R = -1\mu\text{A}$ |
| | | DPAD2,5,10,20,50,100 | -45 | | | |
| | | SSTDPAD5,50,100 | -30 | | | |
| V_F | Forward Voltage | | 0.8 | 1.5 | | $I_F = 1\text{mA}$ |
| $ C_{R1}-C_{R2} $ | Differential Capacitance (ΔC_R) | DPAD1 | | 0.2 | pF | $V_{R1} = V_{R2} = -5\text{V}, f = 1\text{MHz}$ |
| | | ALL OTHERS | | 0.5 | | |
| C_{RSS} | Total Reverse Capacitance | DPAD1 | | 0.8 | pF | $V_R = -5\text{V}, f = 1\text{MHz}$ |
| | | DPAD2,5,10,20,50,100 | | 2.0 | | |
| | | SSTDPAD5,50,100 | | 4.0 | | |

SPECIFIC ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

| SYMBOL | CHARACTERISTIC | DPAD ² | SSTDPAD ² | UNITS | CONDITIONS |
|--------|--|-------------------|----------------------|-------|---------------------|
| I_R | Maximum Reverse Leakage Current ² | (SST)DPAD1 | -1 | pA | $V_R = -20\text{V}$ |
| | | (SST)DPAD2 | -2 | | |
| | | (SST)DPAD5 | -5 | | |
| | | (SST)DPAD10 | -10 | | |
| | | (SST)DPAD20 | -20 | | |
| | | (SST)DPAD50 | -50 | | |
| | | (SST)DPAD100 | -100 | | |

Figure 1. Operational Amplifier Protection

Input Differential Voltage limited to 0.8V (typ) by DPADs D₁ and D₂. Common Mode Input voltage limited by DPADs D₃ and D₄ to ±15V.

Figure 2. Sample and Hold Circuit

Typical Sample and Hold circuit with clipping. DPAD diodes reduce offset voltages fed capacitively from the JFET switch gate.

FIGURE 1

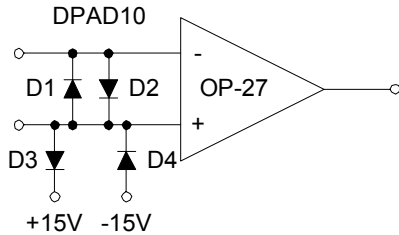
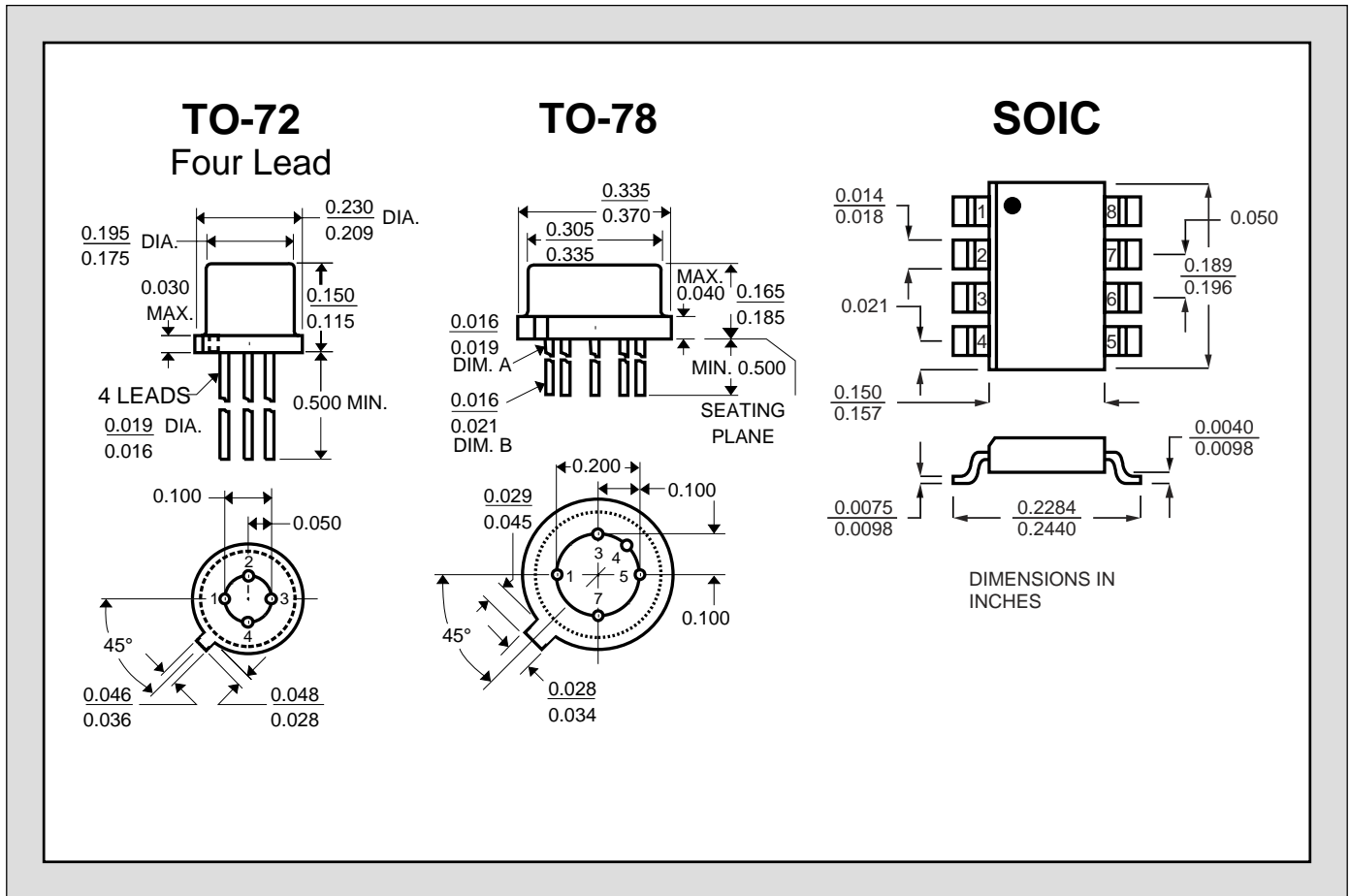
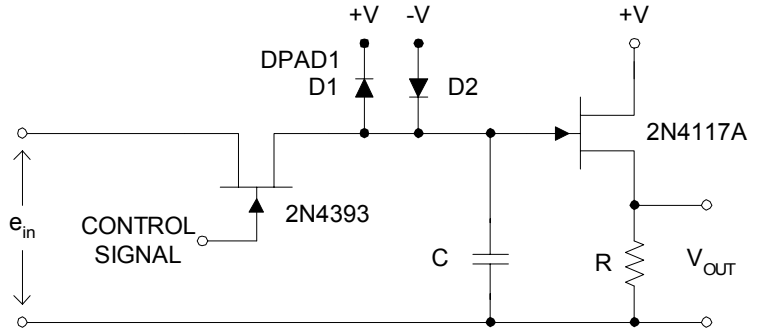


FIGURE 2



1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. The DPAD type number denotes its maximum reverse current value in pico amperes. Devices with I_R values intermediate to those shown are available upon request.

Information furnished by Linear Integrated Systems is believed to be accurate and reliable. However, no responsibility is assumed for its use; nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Linear Integrated Systems.